Remarks

The present amendment responds to the Official Action dated April 10, 2006. A petition for a one month extension of the time to respond and authorization to charge Deposit Account No. 50-1058 the large entity extension fee of $120 accompany this amendment. The Official Action objected to claim 25 as informal. The Official Action rejected claims 24-29 under 35 U.S.C. § 112. The Official Action rejected claims 14, 15 and 19-20 under 35 U.S.C. §102 as being anticipated by Kim et al. U.S. Patent No. 5,542,074 (Kim). Claims 16, 17, and 21-23 were rejected under 35 U.S.C.§103(a) based on Kim in view of Dowling U.S. Patent No. 6,128,728 (Dowling). Claim 18 was rejected under 35 U.S.C. §103(a) based on Kim in view of Sims U.S. Patent No. 6,088,510 (Sims). These grounds of rejection are addressed below.

Claims 1-13 have been previously cancelled without prejudice. Claim 15 is hereby canceled without prejudice and claims 14, 16-19, 21, 24, and 25 have been amended to be more clear and distinct. Claims 14 and 16-29 are presently pending.

The Art Rejections

Kim, Dowling, and Sims do not support the Official Action's reading of them and the rejections based thereupon should be reconsidered and withdrawn. Further, the Applicants do not acquiesce in the analysis of Kim, Dowling, and Sims made by the Official Action and respectfully traverse the Official Action's analysis underlying its rejections.

The Official Action rejected claims 24-29 under 35 U.S.C. § 112. Independent claim 24 has been amended to be more clear and distinct. The S/P bit has been amended to SP/PE-bit as suggested by the Examiner.

The Official Action rejected claims 14, 15, 19 and 20 under 35 U.S.C. §102 as anticipated by Kim. Claim 15 has been canceled making the rejection of claim 15 moot. Regarding the rejected claims 14, 19 and 20, Kim does not teach "at least two processing elements (PEs) and a control processor, where each of the at least two PEs having a set of PE register files and the control processor having a set of control register files, the control processor and at least one PE combined to form a combined processor, wherein the combined processor having substantially similar access to the set of control register files and to the set of PE register files of the at least one PE that was combined to form the combined processor" as presently claimed by claim 14. Rather, Kim teaches that each processing element "consists of a processor 14" and that "register file 46 is a physically integral part of processor 14". Kim makes no mention having "a combined processor" or of a "combined processor having substantially similar access to the set of control register files and to the set of PE register files of the at least one PE that was combined to form the combined processor". Kim's array control unit 20 is separate from the array of PEs as can be seen in Fig. 1 of Kim and Kim provides no motivation to combine the array control unit 20 with a processing element. Kim teaches only a linear array of "identical processing elements" as shown in his Fig. 1, where the PEs are labeled $PE12_1$, $PE12_2$, ..., $PE12_i$, ..., $PE12_N$ "where i is a running integer". Kim, col. 5 lines 34-50 and col. 6, lines 19-20.

As claimed by amended claim 14, a control status bit (CSB) controls whether the array processor operates in an array configuration which matches the physical MxN configuration having "a first operating context stored on the set of control register files", the physical MxN configuration "including the at least one PE of the combined processor" or a compatible operating configuration which corresponds to a different physical OxP configuration, where "O+P<M+N" and having "a second operating context stored on the set of PE register files of the combined processor". For example, referring to Figs. 5A and 5B of the present specification, a 1x5 array processor is illustrated where five processing elements are specified as having a combined SP/PE0 501, PE0/1 551, PE1/2 553, PE2/3 555, and PE3/4 557. This physical configuration of the 1x5 array processor may operate as a 1x5 array processor, where M=1 and N=5, with PEs having physical IDs of 0-4, 501, 551, 553, 555, and 557, when a context status bit (CSB) is inactive. When the CSB is active, the physical configuration of the 1x5 array processor may operate as a 2x2 array processor, where O=2 and P=2, with PEs having virtual IDs 0-3, 551, 553, 555, and 557. It is noted that PE0 is combined with the SP to form the combined SP/PE0 501, in which the physical PE0 is included in the 1x5 organization and not included in the 2x2 organization due to the use of "a second operating context stored on the set of PE register files of the combined processor". See the specification at page 12, lines 9-19, for example. As a result, a software task written for an array processor having a physical OxP (2x2, for example) configuration advantageously executes on the array processor having the physical MxN (1x5, for example) configuration.

It is also noted that Kim's EP register bit is not the same as the CSB bit. Kim's EP bit is used only with an IF-THEN-ELSE statement created from a sequence of instructions received over the IBUS 22 to conditionally execute based on the setting of the EP bit. If an instruction or sequence of instructions is received that are unconditional then all Kim's PEs execute the received instructions "to operate in SIMD mode". Kim, col. 5 lines 41-48 and col. 6, lines 26-29, and col. 9, lines 65-67. However, this aspect of Kim does not meet the CSB as presently claimed by claim 14. The claimed CSB represents two states. Upon detection of the first state, the operating configuration of the array processor matches the physical configuration of the array processor. Upon detection of the second state, the operating configuration of the array processor is different than the physical configuration of the array processor. All instructions, conditional or unconditional execute on the array as configured based on the CSB bit. Claim 14, as presently amended, claims this advantageous operation as follows:

> 14. An array processor comprising:
> a physical MxN array organization of at least two processing elements and a control processor, the at least two processing elements each having a compute register file and the control processor having a control register file, the control processor and at least one processing element combined to form a combined processor, wherein the combined processor having substantially similar access to the control register file and to the compute register file of the at least one processing element that was combined to form the combined processor; and
> a processor state register storing a context status bit (CSB), the CSB having a first state and a second state, the control processor and each processing element operating to detect the state of the CSB,
> the combined processor upon detection of the first state of the CSB operating in a first operating context stored on the control register file, the first operating context adapted for processing a first software task where the first software task is written for an MxN operating configuration which matches the physical MxN array organization including the at least one processing element of

> the combined processor, where M represents the number of rows of processing elements and N represents the number of columns of processing elements,
> the combined processor upon detection of the second state of the CSB operating in a second operating context stored on the compute register file of the combined processor, the second operating context adapted for a second software task where the second software task is written for an OxP operating configuration of the physical MxN array organization where O is the number of rows of processing elements and P is the number of columns of processing elements, the OxP operating configuration not matching the physical MxN array organization as O+P<M+N. (emphasis added)

Claim 19 has been amended in a similar manner to claim 14 placing it in order for allowance.

Claims 16, 17, and 21-23 were rejected under 35 U.S.C.§103(a) based on Kim in view of Dowling. Claim 16 as amended recites the "storing the data contents of the set of PE register files of the combined processor and the PEs in the background while the first software task uses the set of control register files in the foreground, whereby the OxP operating configuration is saved". Dowling does not teach and does not make obvious the "combined processor" or "a context switch from the OxP operating configuration to the MxN operating configuration" as presently claimed. If one hypothetically combined Dowling with Kim, one would expect Dowling's register set 1 and register set 2 to be used in each of Kim's "identical processing elements". Such a combination would do nothing to affect the organization of the linear array of processors.

Claim 17 has been amended in a similar manner to distinctly claim the aspect of restoring the OxP operating configuration from the MxN operating configuration. Claim 17 as presently amended recites:

> 17. The array processor of claim 14 further comprising:
> an eventpoint mechanism to trigger a context switch from the MxN operating configuration to the OxP operating configuration by loading the compute register files of the combined processor and the processing elements in the background with the data contents associated with the OxP operating configuration and after all of the data contents have been loaded, the combined processor switches to the second software task

Dowling does not cure the deficiencies of Kim with respect to the features of this dependent claim.

Claim 18 was rejected under 35 U.S.C. §103(a) based on Kim in view of Sims. Sims does not teach and does not make obvious a combined processor. Sims' micro controller 11 is separate from the processor array 12 as can be seen in Fig. 1 of Sims and Sims provides no motivation to combine the micro controller 11 with a processing element. As a consequence, Sims does not consider the affect of a combined processor on the interpretation of physical identifiers and virtual identifiers. As claimed in amended claim 18, "wherein during the processing of the second software task, instructions are operable in each processing element according to its virtual identifier taking into account the at least one PE that was combined to form the combined processor". Sims does not cure the deficiencies of Kim, and the combination of Kim and Sims does not make this claim obvious.

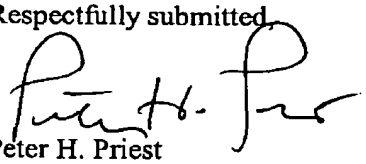
Since dependent claims depend from and contain all the limitations of the amended claims 14 and 19, claims 16-18 and claims 21-23, respectively, distinguish from the references in the same manner as claims 14 and 19 and place claims 16-18 and 21-23 in order for allowance.

Kim, Dowling, and Sims taken separately or in combination, do not teach and do not make obvious different operating configurations of an array processor as presently claimed. In particular, Kim, Dowling, and Sims taken separately or in combination, do not teach and do not suggest, for example, a combined processor, selecting an MxN operating configuration, or an OxP configuration operating on the MxN array organization having a combined processor as presently claimed.

Conclusion

All of the presently pending claims, as amended, appearing to define over the applied references, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,



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